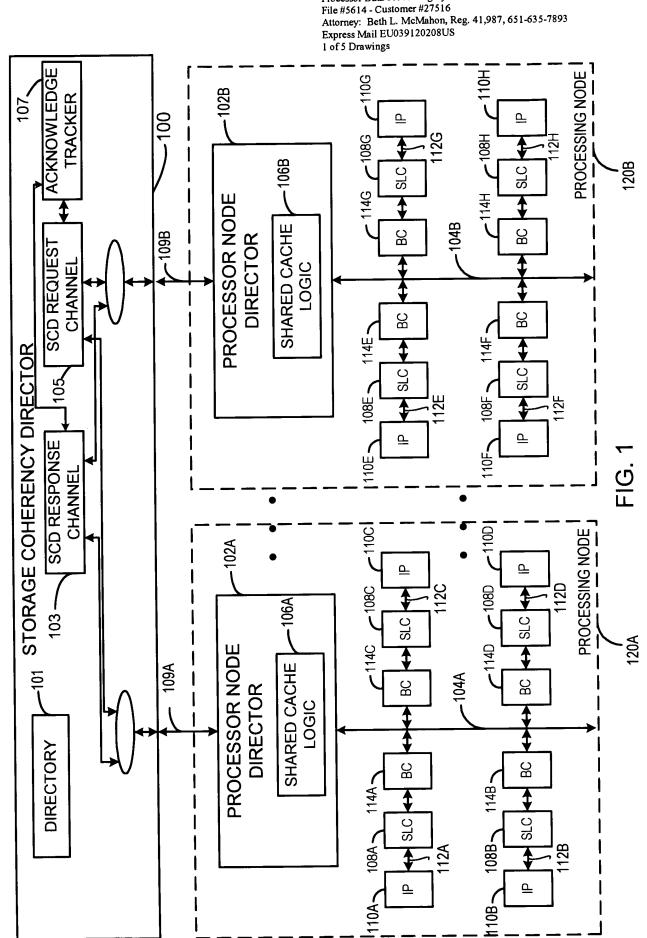
In re Application of Kelvin S. Vartti et al. Title: System and Method for Maintaining Memory Coherency within a Multi Processor Data Processing System File #5614 - Customer #27516



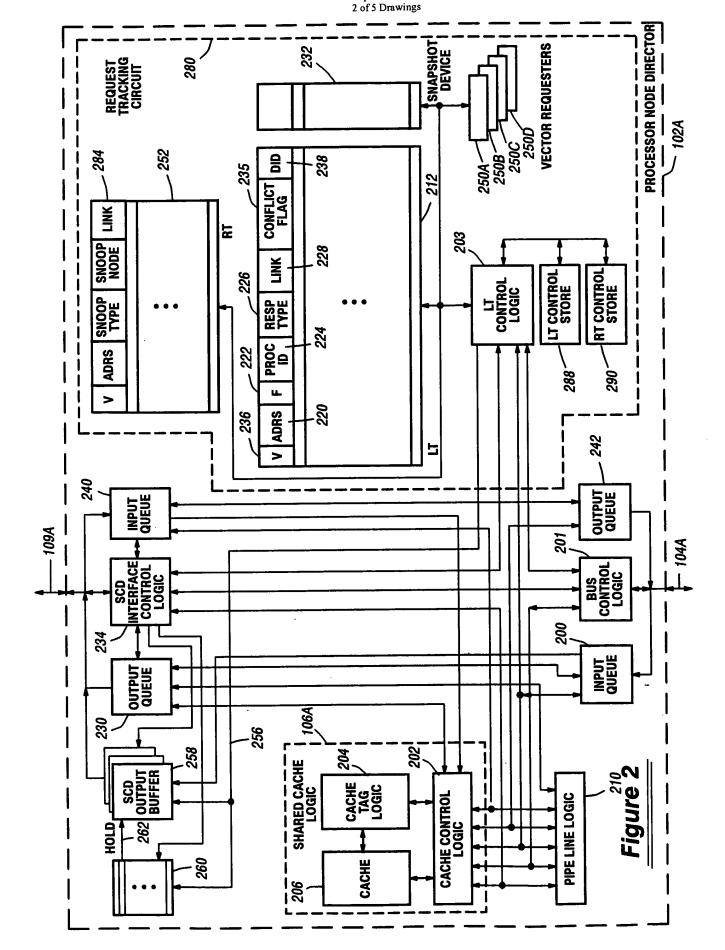
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3 of 5 Drawings 3 of 5 Drawings 114A ထ္ထ 113A SECOND-LEVEL CACHE INVALIDATE REQUESTS PRIMARY INTERFACE 290 -112A **ENZ SIGNAL** 287 281 FIG. 3 284 286 STORAGE DEVICE 285 282 MICROCODE SEQUENCER TAG LOGIC REQUEST STACK MICRO 110A 289 283 292 INSTRUCTION DECODE LOGIC FIRST-LEVEL CACHE INSTRUCTION PROCESSOR

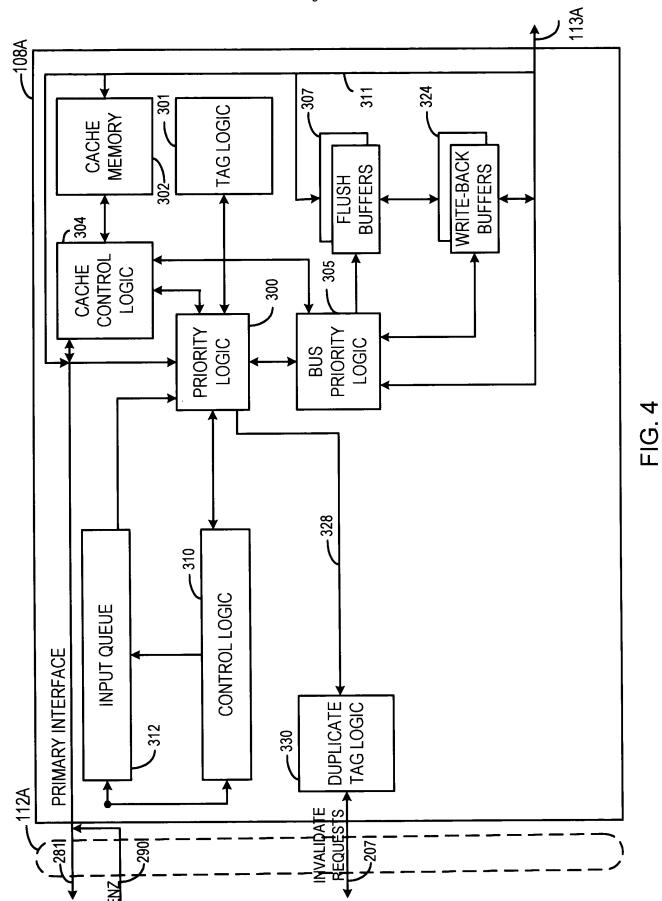
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Processor Data Processing System File #5614 - Customer #27516 Attorney: Beth L. McMahon, Reg. 41,987, 651-635-7893 Express Mail EU039120208US 5 of 5 Drawings *500* PROCESSOR DECODES THE ENZ INSTRUCTION 502 **ACTIVATE ENZ SIGNAL TO THE CACHE** 504 REFERENCE THE CACHE TAG LOGIC WITH THE CACHE LINE ADDRESS PROVIDED BY THE ENZ INSTRUCTION 506 IF A CACHE HIT WITH UNMODIFIED DATA AND READ/WRITE PRIVILEGES OCCURS, INVALIDATE THE CACHE LINE IN THE CURRENT CACHE 508 IF A CACHE HIT WITH MODIFIED DATA OCCURS, FLUSH THE CACHE LINE TO THE NEXT HIGHER MEMORY LEVEL IN THE MEMORY HIERARCHY 510 REQUEST THE CACHE LINE ON THE PROCESSOR BUS, INDICATING THE CURRENT REQUEST IS AN ENZ REQUEST 512 IF A PROCESSOR BUS HIT OCCURS WITH MODIFIED DATA, STORE MODIFIED CACHE LINE IN THE NEXT HIGHER MEMORY LEVEL. THE UNIT MAKING THE REQUEST DISCARDS THE RETURNED CACHE LINE DATA, AND RE-ISSUES THE REQUEST ON THE PROCESSOR BUS 514 IF THE INVALIDATE VECTOR FOR THE PROCESSOR IS NON-ZERO, DEFER THE REQUEST ON THE PROCESSOR BUS 516 CONTINUE WITH STEP 514 UNTIL THE INVALIDATE VECTOR FOR THE PROCESSOR IS CLEARED 518 IS THE REQUESTED CACHE LINE STORED IN THE YES **NEXT HIGHER MEMORY LEVEL?** 520 **↑** NO REQUEST THE CACHE LINE FROM THE MEMORY LEVEL ABOVE THE NEXT HIGHER LEVEL, INDICATING THAT THE REQUEST IS AN ENZ REQUEST 522 DATA IS RETURNED BY ONE OF THE MEMORY LEVELS ABOVE THE NEXT HIGHER MEMORY LEVEL AFTER ALL INVALIDATION OPERATIONS FOR THE CACHE LINE HAVE BEEN COMPLETED 524 RETURN THE CACHE LINE TO THE PROCESSOR SO THAT EXECUTION OF THE ENZ INSTRUCTION COMPLETES, AND THE PROCESSOR MAY EXECUTE THE NEXT INSTRUCTION IN THE INSTRUCTION STREAM 526 PROCESSOR PROVIDES A LOCK RELEASE INDICATION TO THE CACHE, INDICATING THAT THE LOCK SEQUENCE MAY BE CONSIDERED COMPLETED 528 OPTIONALLY, ISSUE IPI TO ANOTHER PROCESSOR IN THE SYSTEM TO SIGNAL THAT DATA INITIALIZED BY THE CURRENT PROCESSOR PRIOR TO **EXECUTION OF ENZ INSTRUCTION MAY BE REFERENCED** Figure 5 DONE

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